



STD50N03L STD50N03L-1

N-CHANNEL 30V - 9.2mΩ - 40A - DPAK/IPAK
STripFET™ III Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STD50N03L	30V	10.5mΩ	40A
STD50N03L-1	30V	10.5mΩ	40A

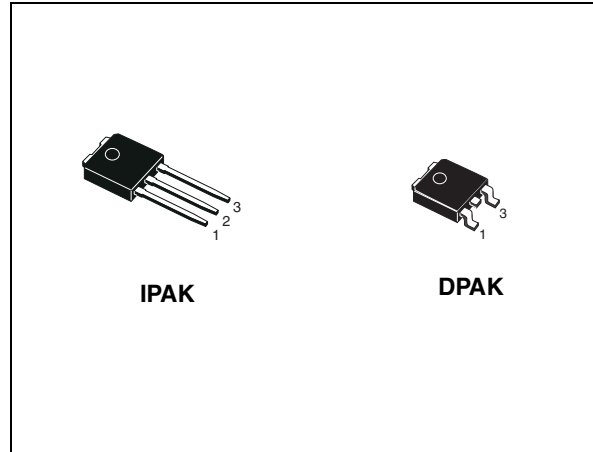
- R_{DS(on)}*Q_g industry's benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold device

Description

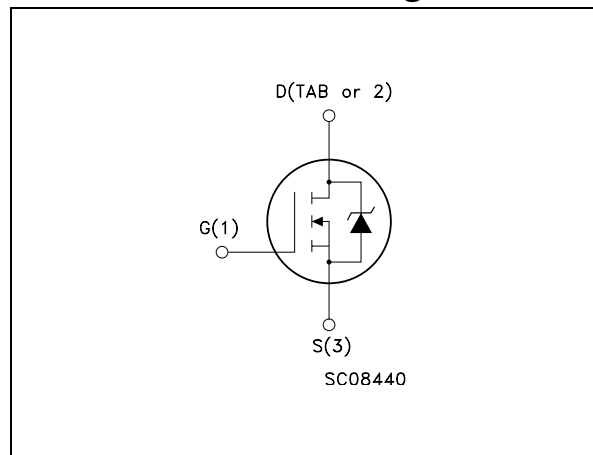
This product utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

Applications

- Switching applications



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STD50N03L	D50N03L	DPAK	Tape & reel
STD50N03L-1	D50N03L	IPAK	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	40	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	36	A
$I_{DM}^{(2)}$	Drain current (pulsed)	160	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	60	W
	Derating factor	0.4	W/ $^\circ\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy	230	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Limited by wire bonding
2. Pulse width limited by safe operating area
3. Starting $T_J = 25^\circ\text{C}$, $I_D = 20\text{A}$, $V_{DD} = 15\text{V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJ-Case}$	Thermal resistance junction-case max	2.5	$^\circ\text{C}/\text{W}$
$R_{thJ-Amb}$	Thermal resistance junction-ambient max	100	$^\circ\text{C}/\text{W}$
T_J	Maximum lead temperature for soldering purpose	275	$^\circ\text{C}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 30\text{V}$ $V_{DS} = 30\text{V}$, $T_C=125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 20\text{A}$ $V_{GS} = 5\text{V}$, $I_D = 20\text{A}$		9.2 0.012	10.5 0.019	$\text{m}\Omega$ Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		1434 294 48		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 15\text{V}$, $I_D = 40\text{A}$ $V_{GS} = 5\text{V}$ (see Figure 13)		10.4 5.1 3.7	14	nC nC nC
$Q_{OSS}^{(1)}$	Output charge	$V_{DS} = 24\text{V}$; $V_{GS} = 0$		12.6		nC
R_G	Gate input resistance	$f = 1\text{MHz}$ Gate Bias Bias=0 Test signal Level=20mV open drain		1.1		Ω

1. $Q_{OSS} = C_{OSS} \cdot D \cdot V_{in}$; $C_{OSS} = C_{gd} + C_{gd}$. See [Appendix A](#)

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=15V$, $I_D=25A$, $R_G=4.7\Omega$, $V_{GS}=4.5V$ (see Figure 12)		15 125		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=15V$, $I_D=25A$, $R_G=4.7\Omega$, $V_{GS}=4.5V$ (see Figure 12)		14 45		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				40 160	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=20A$, $V_{GS}=0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=40A$, $di/dt=100A/\mu s$, $V_{DD}=10V$, $T_j=25^\circ C$ (see Figure 17)		26 15.6 1.2		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=40A$, $di/dt=100A/\mu s$, $V_{DD}=10V$, $T_j=150^\circ C$ (see Figure 17)		26.4 18.1 1.4		ns nC A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

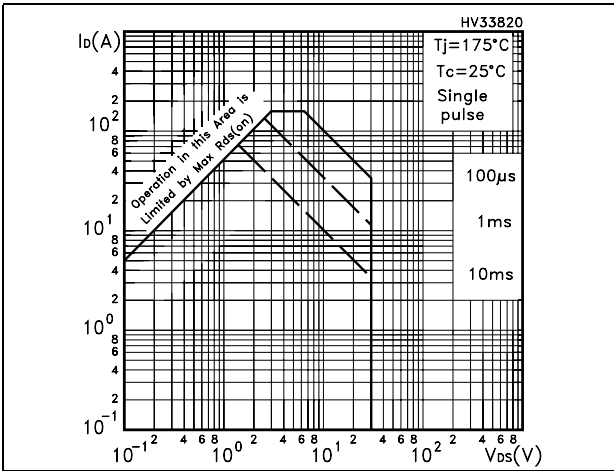


Figure 2. Thermal impedance

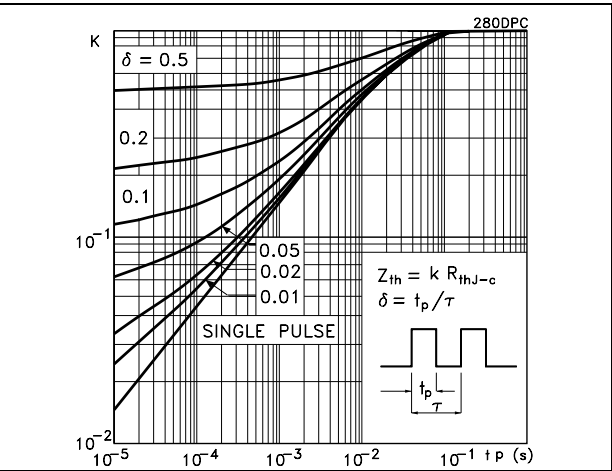


Figure 3. Output characteristics

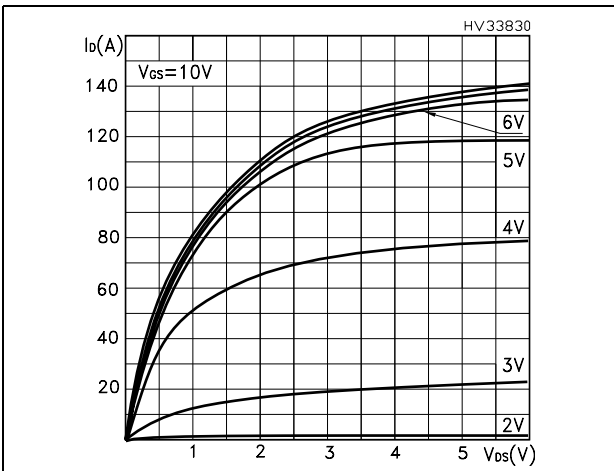


Figure 4. Transfer characteristics

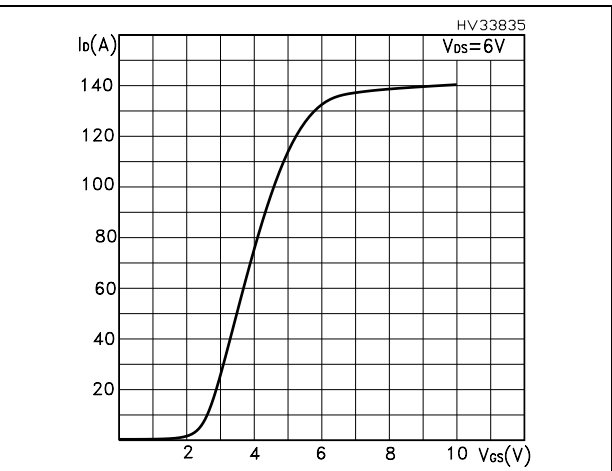


Figure 5. Normalized BvDSS vs temperature

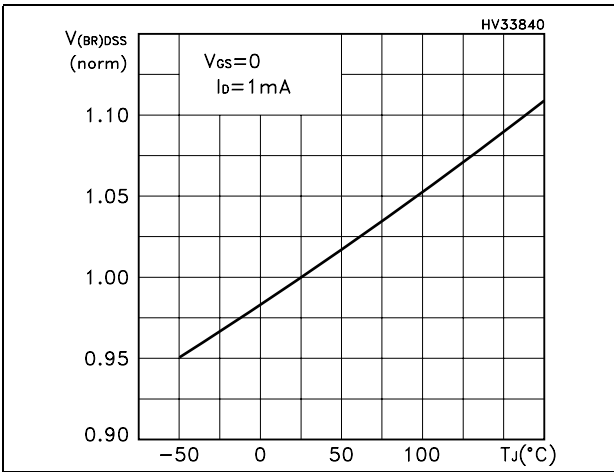


Figure 6. Static drain-source on resistance

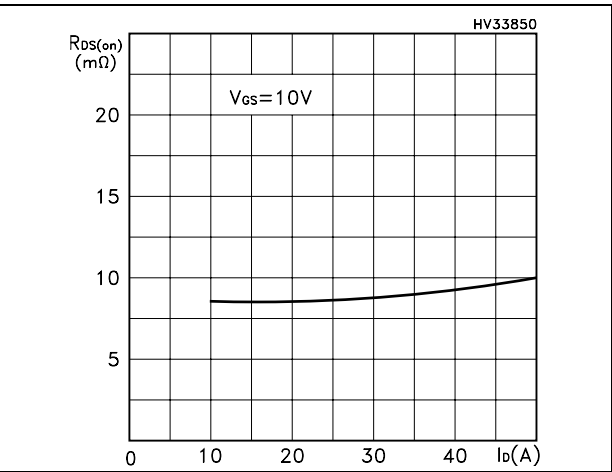


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

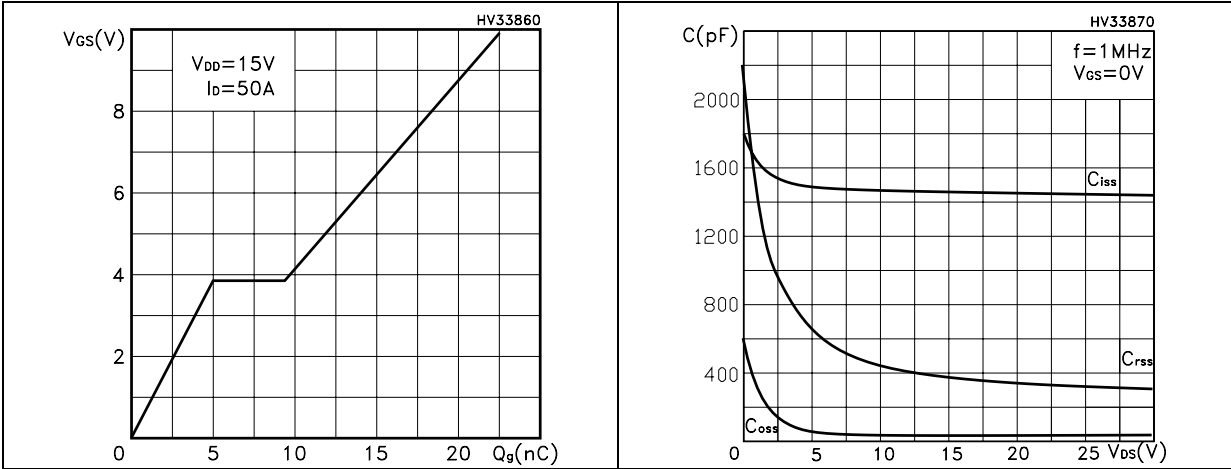


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

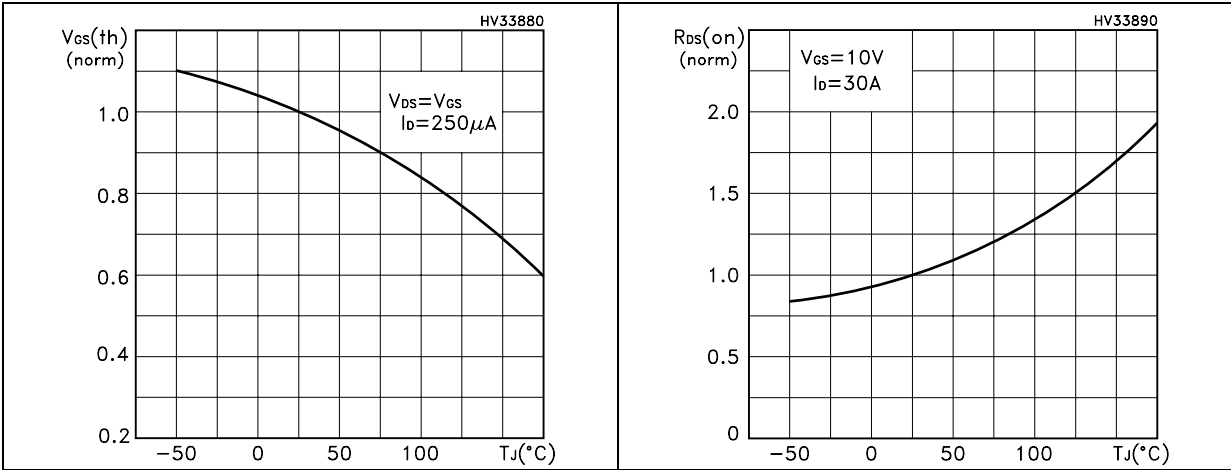
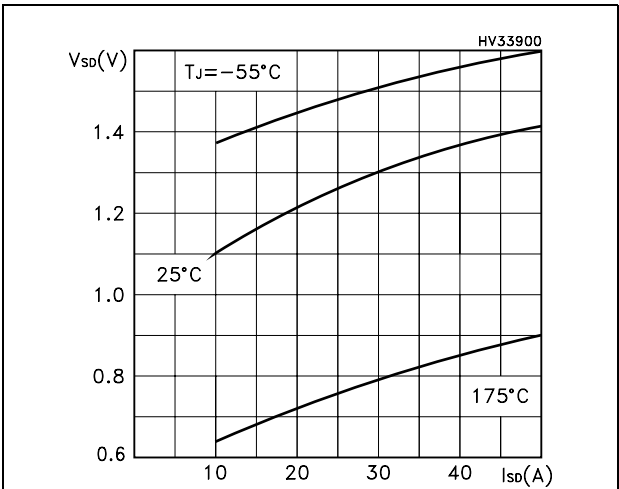


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

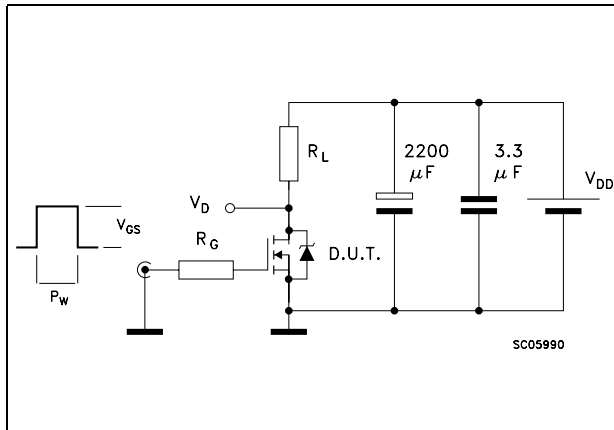


Figure 13. Gate charge test circuit

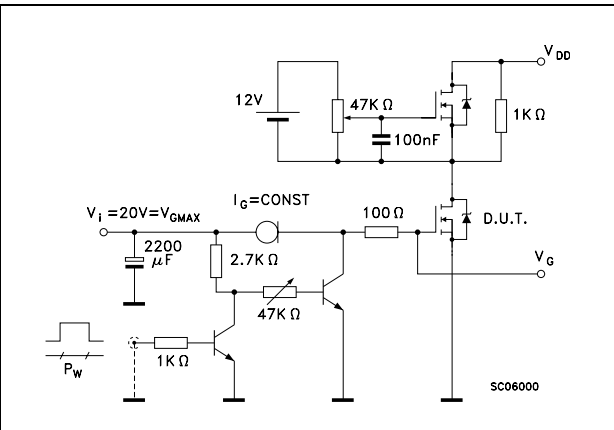


Figure 14. Test circuit for inductive load switching and diode recovery times

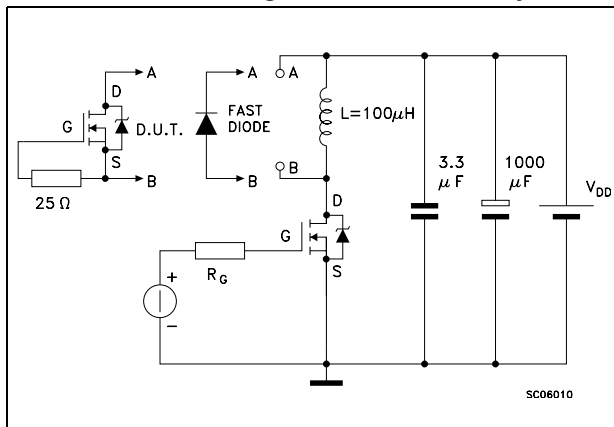


Figure 15. Unclamped Inductive load test circuit

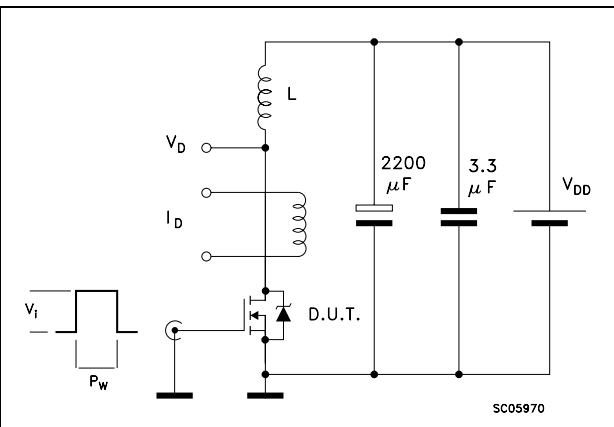


Figure 16. Unclamped inductive waveform

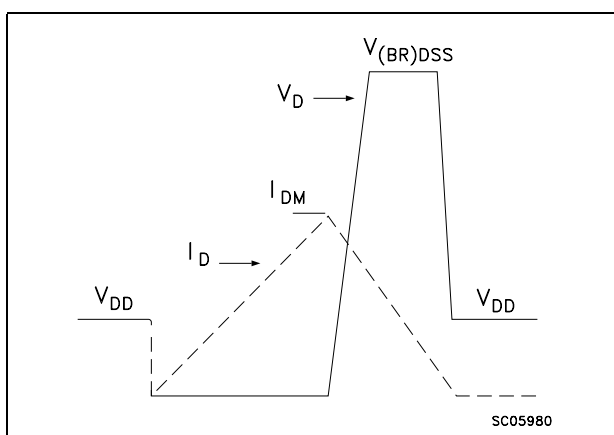
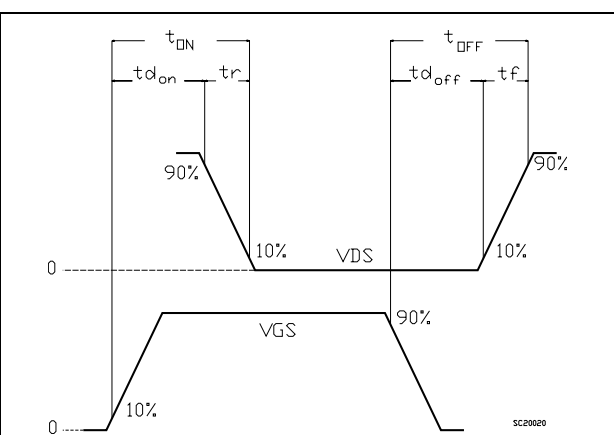
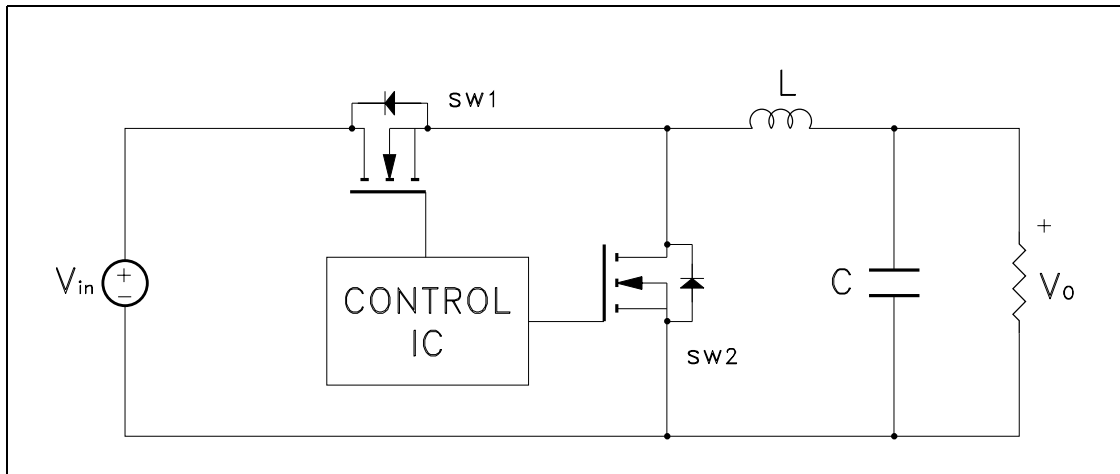


Figure 17. Switching time waveform



Appendix A Buck converter

Figure 18. Power losses estimation



The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (SW2) device requires:

- Very low $R_{DS(on)}$ to reduce conduction losses
- Small Q_{gl} s to reduce the gate charge losses
- Small C_{oss} to reduce losses due to output capacitance
- Small Q_{rr} to reduce losses on SW1 during its turn-on
- The C_{gd}/C_{gs} ratio lower than V_{th}/V_{gg} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;

The high side (SW1) device requires:

- Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Q_g to have a faster commutation and to reduce gate charge losses

Low $R_{DS(on)}$ to reduce the conduction losses.

Table 7. Power losses

		High side switching (SW1)	Low side switch (SW2)
$P_{\text{conduction}}$		$R_{\text{DS(on)SW1}} * I_L^2 * \delta$	$R_{\text{DS(on)SW2}} * I_L^2 * (1 - \delta)$
$P_{\text{switching}}$		$V_{\text{in}} * (Q_{\text{gsth(SW1)}} + Q_{\text{gd(SW1)}}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
P_{diode}	Recovery (1)	Not applicable	$V_{\text{in}} * Q_{\text{rr(SW2)}} * f$
	Conduction	Not applicable	$V_{\text{f(SW2)}} * I_L * t_{\text{deadtime}} * f$
$P_{\text{gate(QG)}}$		$Q_{\text{g(SW1)}} * V_{\text{gg}} * f$	$Q_{\text{gls(SW2)}} * V_{\text{gg}} * f$
P_{Qoss}		$\frac{V_{\text{in}} * Q_{\text{oss(SW1)}} * f}{2}$	$\frac{V_{\text{in}} * Q_{\text{oss(SW2)}} * f}{2}$

1. Dissipated by SW1 during turn-on

Table 8. Paramiters meaning

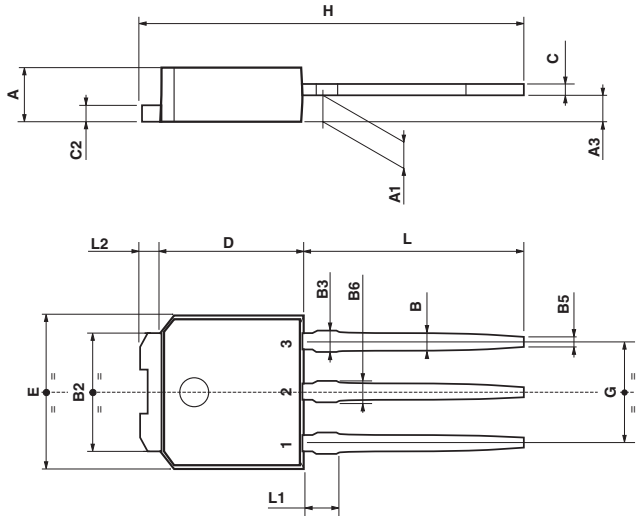
Parameter	Meaning
d	Duty-cycle
Q_{gsth}	Post threshold gate charge
Q_{gls}	Third quadrant gate charge
$P_{\text{conduction}}$	On state losses
$P_{\text{switching}}$	On-off transition losses
P_{diode}	Conduction and reverse recovery diode losses
P_{gate}	Gate drive losses
P_{Qoss}	Output capacitance losses

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : www.st.com

TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



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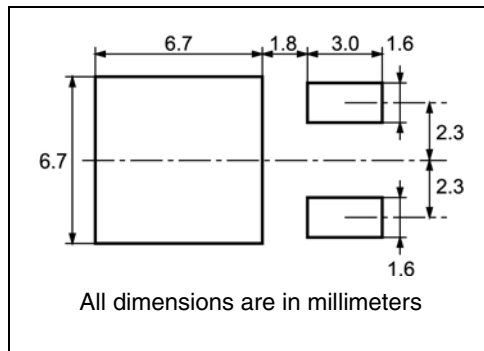
DPAK MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

The mechanical drawing illustrates the STD50N03L DPAK package. It includes a top view showing dimensions E, b4, L2, L4, H, e, e1, and b(2x). A side view shows dimensions A, A1, A2, C2, D, D1, E1, L, L1, L2, L4, R, and V2. A detail view of the thermal pad shows dimensions E1, D1, and L1. The drawing also indicates the SEATING PLANE and GAUGE PLANE, with a 0.25mm dimension for the gauge plane.

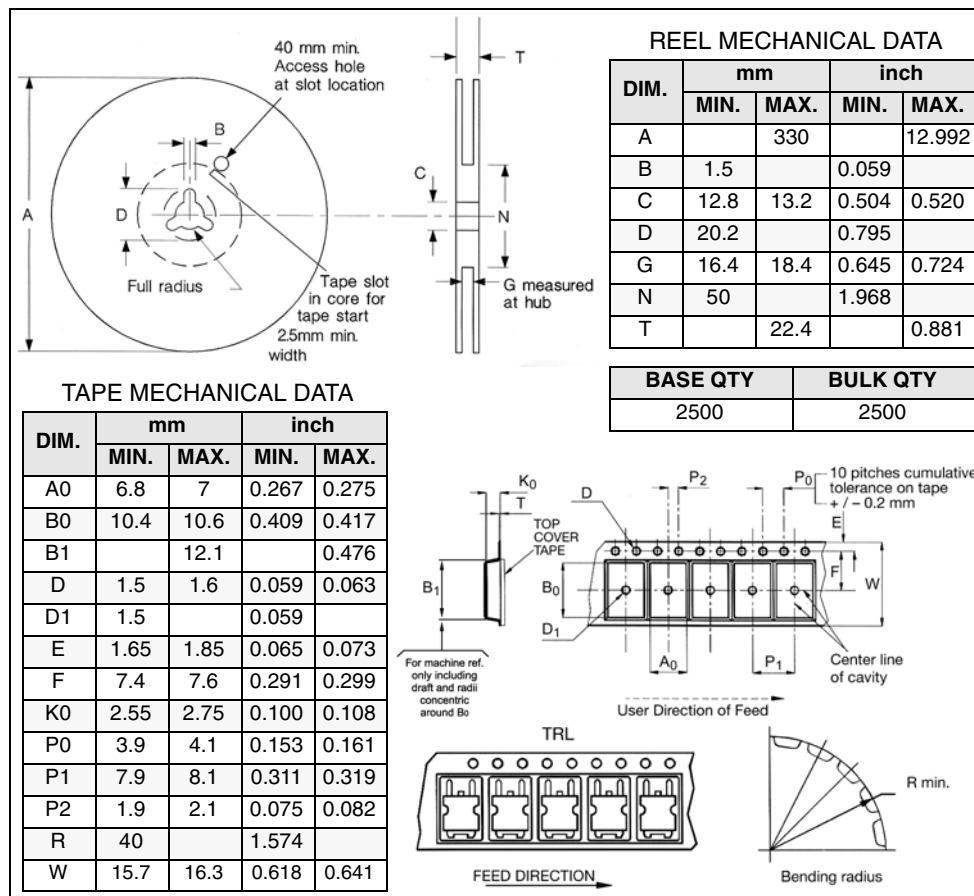
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5 Packaging mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 9. Revision history

Date	Revision	Changes
31-Jul-2006	1	Initial release.
27-Oct-2006	2	Modified <i>Figure 1.: Safe operating area on page 6</i>

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